EE 505

Lecture 24

ADC Design

– Pipeline

Review from last lecture

How Much Gain?

Depends upon how much of the overall error budget is allocated to the effect noninfinite gain has on required performance parameters

If require n $ENOB_{INL}$, can the ½ LSB error be allocated to effects of op amp gain error?

e.g. If INL specification of a 12-bit ADC is ½ LSB, can ½ LSB be allocated to the noninfinite gain error?

Sources that may contribute to INL errors in pipelined ADC:

Finite Op Amp Gain
Capacitor Missmatch
Incomplete amplifier settling
Amplifier nonlinearity
Input S/H error
Parasitic capacitance nonlinearity
Offset voltage (in ADC, DAC, summer)
DAC errors
ADC nonlinaritry

Review from last lecture

Error Budgeting

Sources that may contribute to INL errors in pipelined ADC:

Finite Op Amp Gain
Capacitor Missmatch
Incomplete amplifier settling
Amplifier nonlinearity
Input S/H error
Parasitic capacitance nonlinearity
Offset voltage (in ADC, DAC, summer)
DAC errors
ADC nonlinaritry

If entire error budget (e.g. ½ LSB) is allocated to the Finite Op Amp Gain, what error budget must be allocated to all remaining contributors?

All other contributors must each contribute 0 LSB

What will happen if each error source is allocated an error budget of (e.g. ½ LSB)?

ENOB will probably be 2 or 3 bits less than required

How should the error sources contribution to overall error budget be allocated?

$$\sum_{i=1}^{m} e_i = \frac{1}{2} LSB$$ (maybe a little bit overly conservative)

In a way that will minimize design effort and die area

A bit overly conservative because the random parts of the errors often uncorrelated

Review from last lecture

What type of error budget is used by industry?

Is ENOB equal to the specified number of bits of resolution?

Is it easy to add one additional ENOB of resolution to a given design ?

Why is the ENOB often less than the specified number of bits?

Will consider one example only, others may have ENOB closer or farther from specified resolution

Review from last lecture

Can we depend on this "13-bit" INL performance?

SPECIFICATIONS

AVDD1 = 1.8 V, AVDD2 = 3.3 V, AVDD3 = 1.8 V, DRVDD = 1.8 V, specified maximum sampling rate, 2.5 V p-p differential input, 1.25 V internal reference, AIN = −1.0 dBFS, DCS on, default SPI settings, unless otherwise noted.

Table 1.

Parameter[1]	Temp	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ACCURACY					
No Missing Codes	Full		Guaranteed		
Offset Error	Full	−200	0	+200	LSB
Gain Error	Full	−3.9	−0.1	+2.6	%FSR
Differential Nonlinearity (DNL)[2]	Full	−0.9	±0.5	+1.5	LSB
Integral Nonlinearity (INL)[2]	Full	−12	±3.5	+12	LSB
TEMPERATURE DRIFT					
Offset Error	Full		±0.023		%FSR/°C
Gain Error	Full		±0.036		%FSR/°C
ANALOG INPUTS					
Differential Input Voltage Range (Internal VREF = 1 V to 1.25 V)	Full	2	2.5	2.5	V p-p
Common-Mode Voltage	25°C		2.15		V
Differential Input Resistance	25°C		530		Ω
Differential Input Capacitance	25°C		3.5		pF
Full Power Bandwidth	25°C		900		MHz
XVREF INPUT					
Input Voltage	Full	1		1.25	V
Input Capacitance	Full		3		pF
POWER SUPPLY					
AVDD1	Full	1.75	1.8	1.85	V
AVDD2	Full	3.0	3.3	3.6	V
AVDD3	Full	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	V
I_{AVDD1}	Full		567	620	mA
I_{AVDD2}	Full		55	61	mA
I_{AVDD3}	Full		31	35	mA
I_{DRVDD}	Full		40	43	mA
Total Power Dissipation (Including Output Drivers)	Full		1.33	1.5	W
Power-Down Dissipation	Full		4.4	90	mW

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions and how these tests were completed.
[2] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.

$\log_2(12)=3.58$

$$\text{ENOB} = n_R\text{-}1\text{-}\log_2(\upsilon) = 16 - 1 - 3.58 \cong 11.42$$

From INL viewpoint, performance of marketed parts could be about 4.5 bits less than physical resolution but does have other attractive properties

Review from last lecture

How Much Gain?

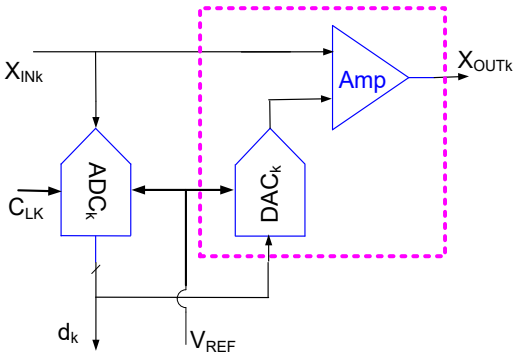
Conventional Approach: Assume want to make at most ½ LSB error in closed loop gain at each stage

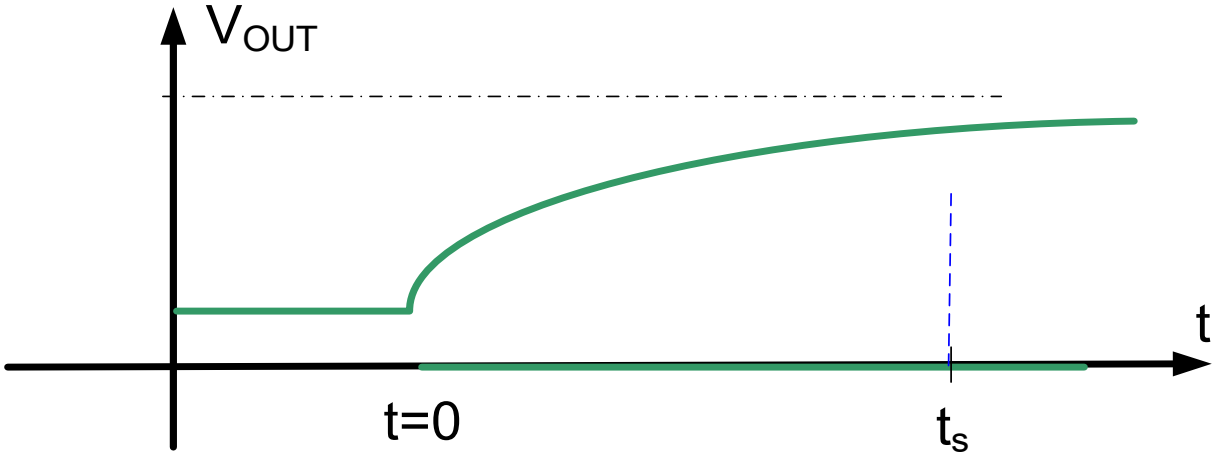
Often see authors use $A_{dB} \cong 6n_{ST} + 12$

- Gives no information about drop in gain at boundary of input/output window
- Not dependent upon architecture ?
- Maybe uses too much error budget on gain
- Errors accumulate since gain errors will exist on each stage
- No indication how A_{dB} relates to INL or DNL
- Gain requirements are large on the input buffer (n_{ST}=n) but will be significantly relaxed on latter stages in the pipeline when n_{ST} decreases

Review from last lecture

Amplifier Settling Time





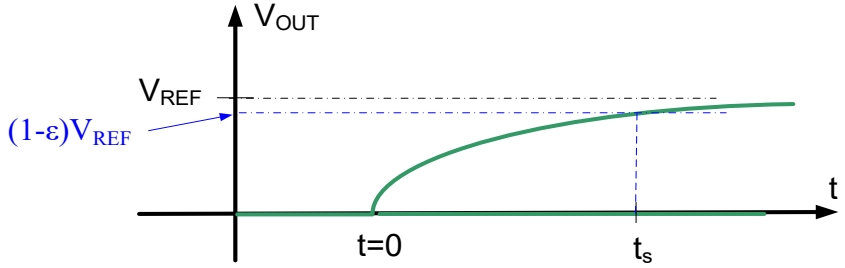
- Can show that no distortion is introduced in pipelined ADC if the amplifier settling is linear (i.e. don't worry about incomplete settling)
- But invariably slew rate and op amp nonlinearities will cause settling to be nonlinear
- Since can't guarantee linear settling, must design for complete settling

Review from last lecture

Settling Time

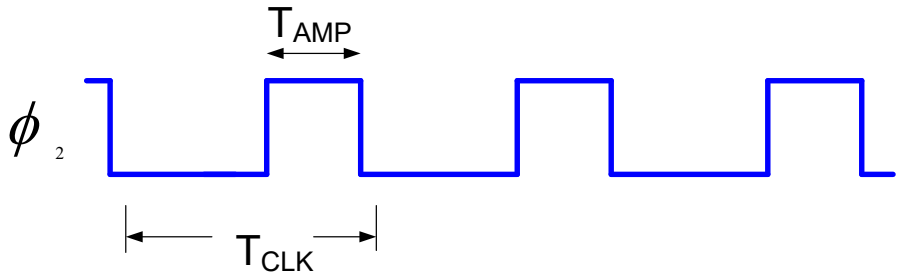
Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step in each stage

Step response (if slewing is neglected)



Design requirements for GB of Op Amp

$$t_s \cong \frac{0.7(n_{ST}+1)}{\beta GB}$$



$$t_s = t_{AMP} \cong \frac{T_{CLK}}{2} = \frac{1}{2f_{CLK}}$$

$$GB_{RPS} \cong \frac{1.4(n_{ST}+1)}{\beta} f_{CLK}$$

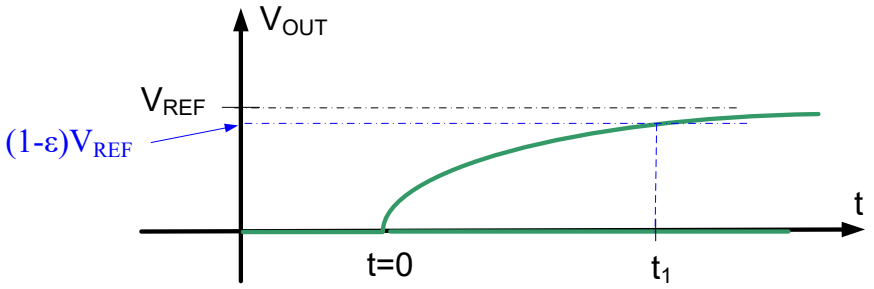
$$GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

Note: GB requirements drop from stage to stage

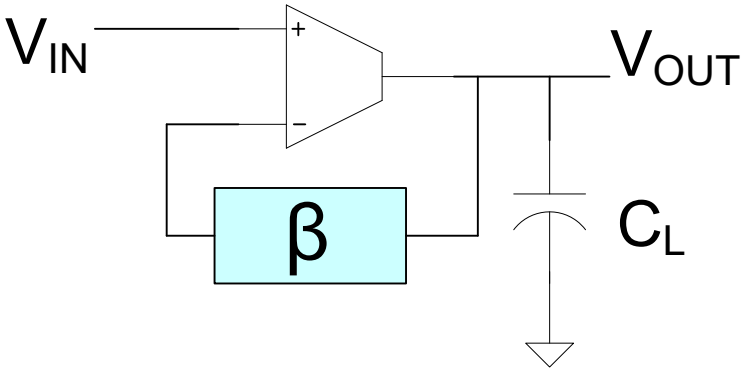
Review from last lecture

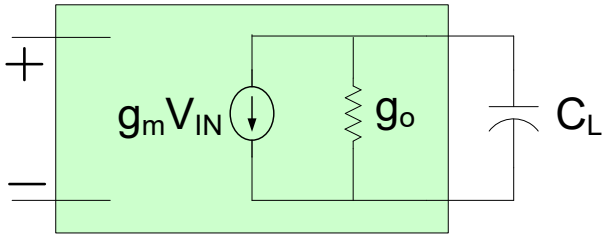
Settling Time

Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step



What about high-impedance op amp?





$$A_{OL} = -\frac{g_m}{g_o} \qquad BW = \frac{g_o}{C_L} \qquad GB = \frac{g_m}{C_L}$$

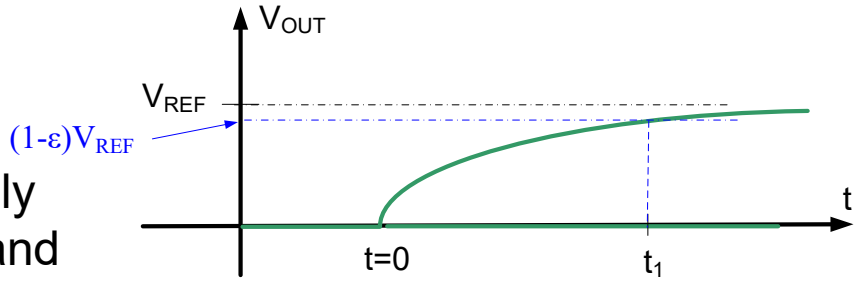
$$A_{FB} = \frac{g_m}{sC_L + g_o + \beta g_m} \cong \frac{g_m}{sC_L + \beta g_m} = \frac{GB}{s + \beta GB}$$

Note this is identical in form to that from the internally compensated op amp

Settling Time

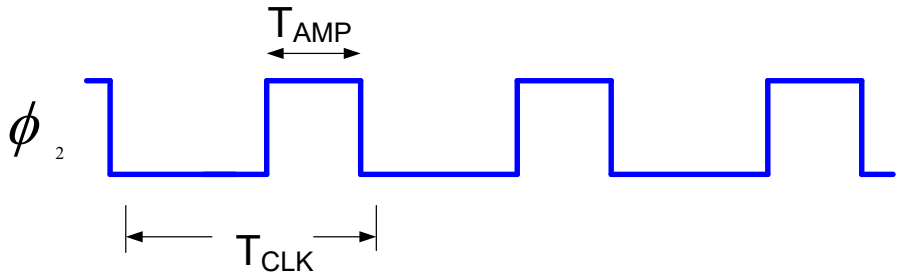
Conventional Approach: Assume want to make at most ½ LSB error in settling for worst-case step

Step response (if slewing is neglected)



Design requirements for GB of Op Amp apply to both compensated two-stage structures and high output impedance single-stage structures

$$t_s \cong \frac{0.7(n_{ST}+1)}{\beta GB}$$



$$t_s = t_{AMP} \cong \frac{T_{CLK}}{2} = \frac{1}{2f_{CLK}}$$

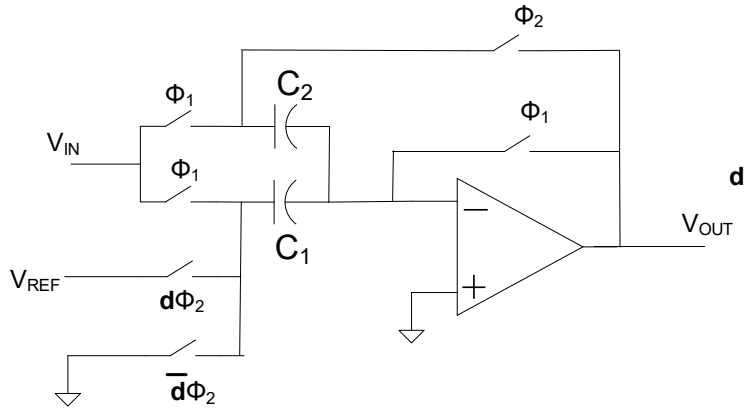
$$GB_{RPS} \cong \frac{1.4(n_{ST}+1)}{\beta} f_{CLK}$$

$$GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

Notes: May be over-using error budget
Slewing will modestly slow response

How Much Gain Revisted ?

Conventional Approach: Assume want to make at most ½ LSB error in closed loop gain at each stage



Often see authors use

$$A_{dB} \cong 6n_{ST} + 12$$

$$\beta = \frac{C_2}{C_1 + C_2}$$

$$A_{FB} = \frac{\frac{C_1}{C_1 + C_2} A}{1 + A\frac{C_2}{C_1 + C_2}} \Rightarrow A_{FB} = \frac{(1-\beta)A}{1 + A\beta}$$

How Much Gain Revisted ?

Conventional Approach: Assume want to make at most ½ LSB error in closed loop gain at each stage

$$A_{FB} = \frac{(1-\beta)\mathrm{A}}{1+\mathrm{A}\beta} \quad \Rightarrow \quad \Delta\mathrm{A}_{\mathrm{FB}} = \frac{(1-\beta)\mathrm{A}}{1+\mathrm{A}\beta} - \frac{1-\beta}{\beta} \simeq \frac{-(1-\beta)}{\beta^2 A}$$

Observe: $n = \sum_{i=1}^{m} n_i$ where n_i is the number of bits on stage i

Consider initially first stage errors:

Assume want to set gain A so that worst case error in output residue at the output of stage 1 deviates by at most θ_1 LSB

- 1 LSB error in residue at output of the first stage is $1\ \frac{LSB}{2^{n_1}}$
- Input that causes worst case error is $V_{IN\_WC} = \frac{V_{REF}}{2^{n_1}}$

How Much Gain Revisted ?

Conventional Approach: Assume want to make at most ½ LSB error in closed loop gain at each stage

- 1 LSB error in residue at output of the first stage is $1\ \frac{LSB}{2^{n_1}}$
- Input that causes worst case error is $V_{IN\_WC} = \frac{V_{REF}}{2^{n_1}}$

$$V_{OUT\_DES} = V_{IN\_WC}\frac{1-\beta}{\beta} = \frac{V_{REF}}{2^{n_1}}\frac{1-\beta}{\beta}$$

$$V_{OUT\_ACT} = V_{IN\_WC}A_{FB} = V_{IN\_WC}\frac{(1-\beta)\mathrm{A}}{1+\mathrm{A}\beta}$$

Thus

$$\Delta V_{OUT\_MAX} = \mathrm{V}_{\mathrm{OUT\_ACT}} - \mathrm{V}_{\mathrm{OUT\_DES}}$$

Which can be expressed as:

$$\Delta V_{OUT\_MAX} \simeq -\frac{V_{REF}}{2^{n_1}}(1-\beta)\frac{1}{\mathrm{A}\beta^2}$$

How Much Gain Revisted ?

Conventional Approach: Assume want to make at most ½ LSB error in closed loop gain at each stage

$$\Delta V_{OUT\_MAX} \simeq -\frac{V_{REF}}{2^{n_1}}(1-\beta)\frac{1}{A\beta^2}$$

Error Budget for First Stage: θ_1 LSB ⇒ $\Delta V_{OUT\_MAX} \le \theta_1 LSB$

$$\frac{V_{REF}}{2^{n_1}}(1-\beta)\frac{1}{A\beta^2} \le \theta_1 \frac{V_{LSB}}{2^{n_1}}$$

Solving for A we obtain:

$$A \ge 2^n \frac{(1-\beta)}{\theta_1\beta^2} \Rightarrow A_{dB} \ge 6n + 20\log\left(\frac{1-\beta}{\theta_1\beta^2}\right)$$

Note: A dependent upon n, β, and θ_1 and not dependent on n_1 (but β dependent upon n_1)

How Much Gain Revisted ?

Conventional Approach: Assume want to make at most ½ LSB error in closed loop gain at each stage

$$A_{dB} \geq 6n + 20\log\left(\frac{1-\beta}{\theta\beta^2}\right)$$

Example: 1-bit/stage architecture with $\theta_1 = \frac{1}{4}$

$$A_{dB} \geq 6n + 18$$

Note this is significantly larger than the rule of the thumb

If $\theta_1 = \frac{1}{2}$ obtain $A_{dB} \geq 6n + 12$

Analysis a bit conservative because the average error would probably be about ½ of the WC error

Regardless, rule of the thumb is putting almost all error budget in op amp gain error!

How Much Gain Revisted ?

For an m-stage pipeline, it follows that

$$A_k \geq 2^{n+\sum_{i=1}^{k-1} n_i} \frac{1-\beta_k}{\theta_k \beta_k^2} \qquad 1 \leq k \leq m-1$$

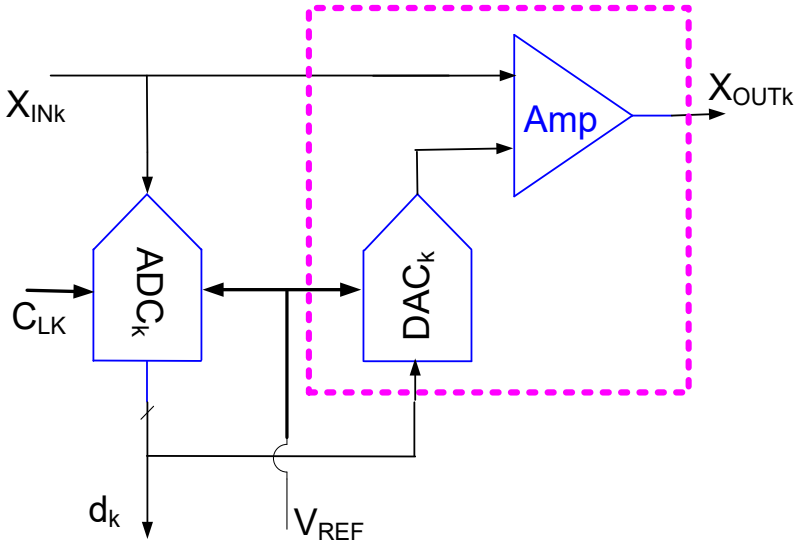
Total worst-case gain error for m-stage pipelined ADC

$$\theta_{TOT} = \sum_{i=1}^{m} \theta_i$$

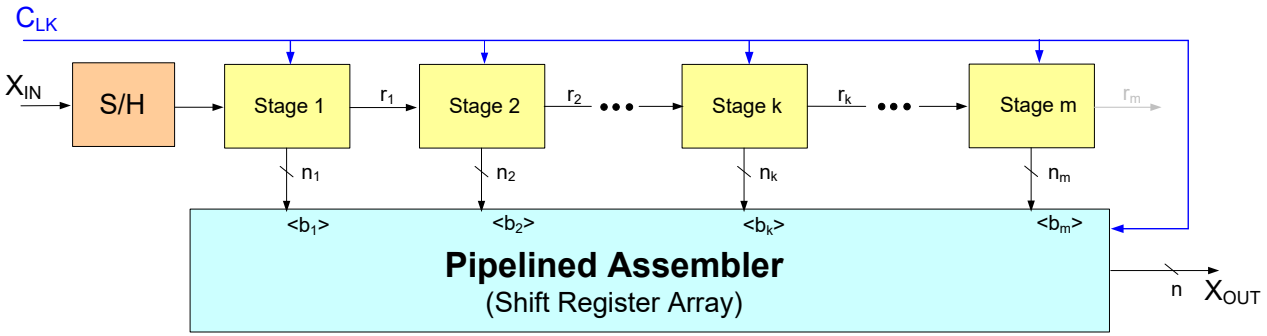
May be somewhat conservative since WC errors will seldom occur on each stage at same time

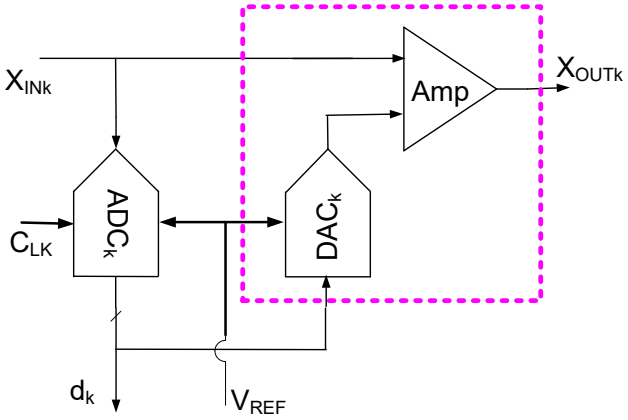
Performance Limitations
(consider amplifier, ADC and DAC issues)

- ADC
  - Break Points (offsets)
- DAC
  - DAC Levels (offsets)
    - Out-range (over or under range)
- Amplifier
  - Offset voltages
- Settling Time
  - Nonlinearity (primarily open loop)
    - Open-loop
    - Out-range
  - Gain Errors
    - Component mismatch
    - Inadequate open loop gain
- Power Dissipation
  - kT/C switching noise



Power Dissipation

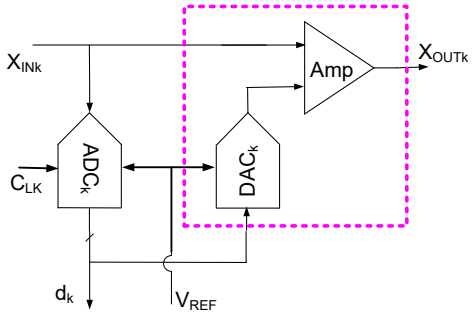




Dominant source of power dissipation is in the op amps in S/H and individual stages

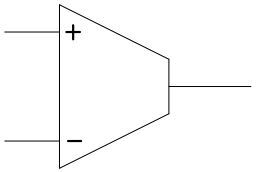
Power Dissipation

- Power dissipation strongly dependent upon op amp architecture and design
- Power budgets critical and even a net 5% savings in power is significant!



Consider a single stage in the pipeline

Consider single stage open-loop op amp structures (e.g. telescopic cascode)

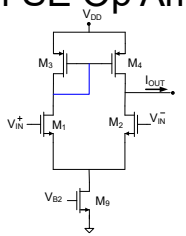


$$A_{OL} = -\frac{g_{mT}}{g_{oT}}$$

$$P_{OP\ AMP} \cong 2I_{DQ}\left(V_{DD} - V_{SS}\right)$$

Power increases linearly with I_{DQ}

Ref SE Op Amp



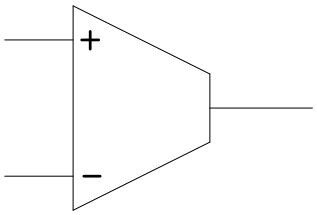
For MOS implementation with basic reference SE op amp

$$A_{OL} = -\frac{2I_{DQ}}{V_{EB}}\frac{1}{2\lambda I_{DQ}} = -\frac{1}{\lambda V_{EB}}$$

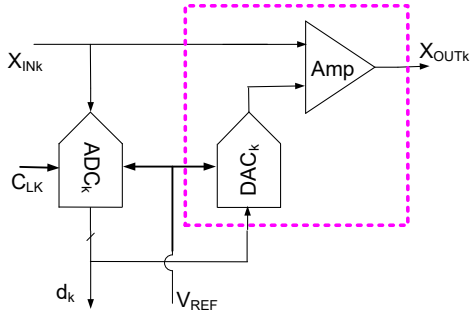
No power implications on dc gain of op amp

- Pick V_{EB} small to increase gain
- Keep lengths larger than minimum to make λ small

Power Dissipation



$$GB = \frac{g_{mT}}{C_L}$$



C_L is the parallel combination of any interconnect capacitance, the capacitance of the β network and the sampling capacitance of the following stage

For MOS implementation (with ref SE op amp or telescopic cascode op amp)

$$GB = \frac{2I_{DQ}}{V_{EB}C_L} = \left(\frac{1}{(V_{DD}-V_{SS})}\frac{P}{C_L}\right)\frac{1}{V_{EB}}$$

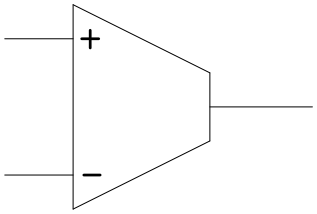
For convenience, define

$$V_{SUP} = V_{DD} - V_{SS}$$

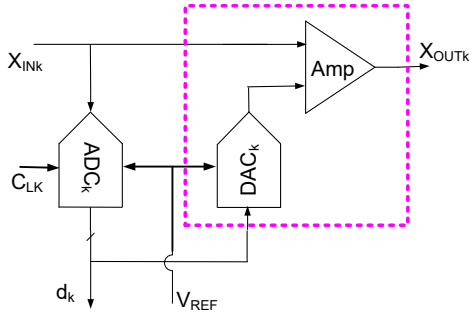
$$P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB}$$

- P increases linearly with GB
- Keep V_{EB} small, C_L as small as possible, GB as small as possible
- At high speeds, diffusion parasitics will cause P to increase more rapidly than GB
- Total amplifier power is sum of power in each stage

Power Dissipation

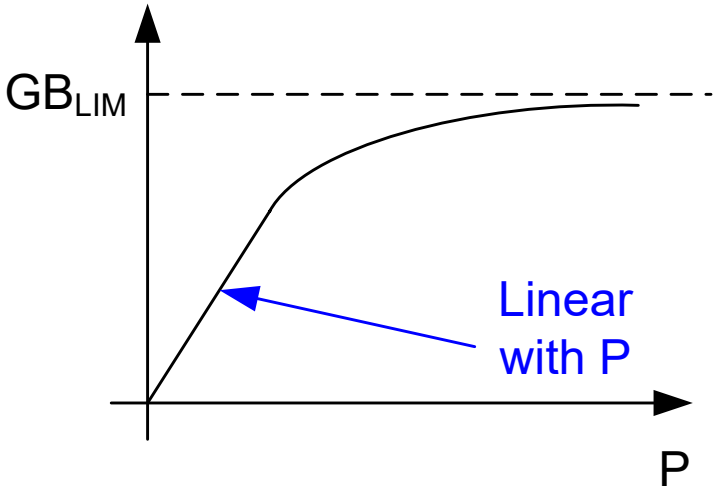


$$GB = \frac{g_m}{C_L}$$



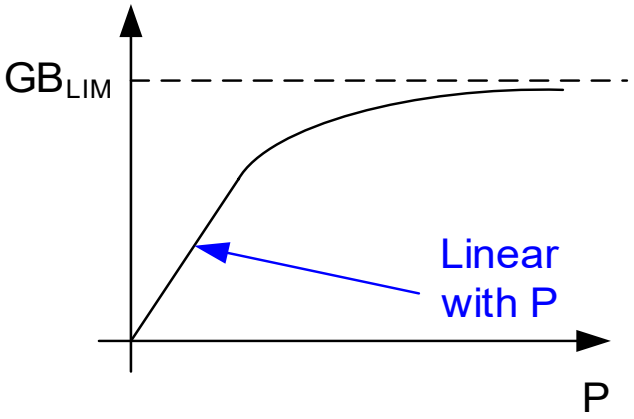
For single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

$$P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB}$$

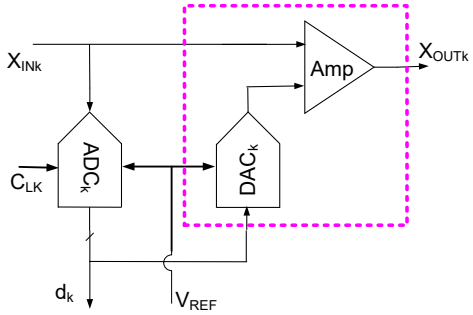


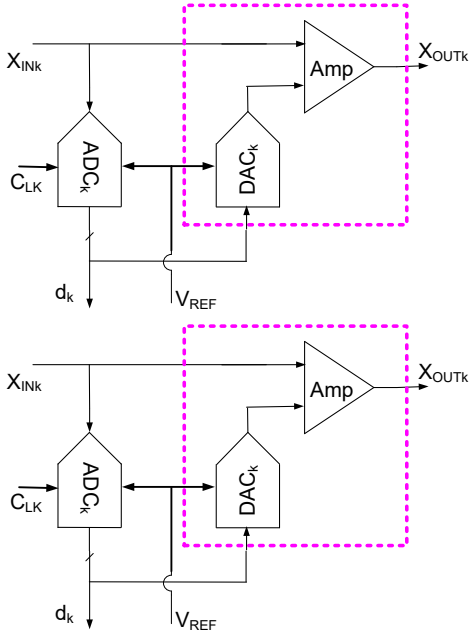
At high speeds, diffusion parasitics will cause P to increase more rapidly than GB

Power Dissipation



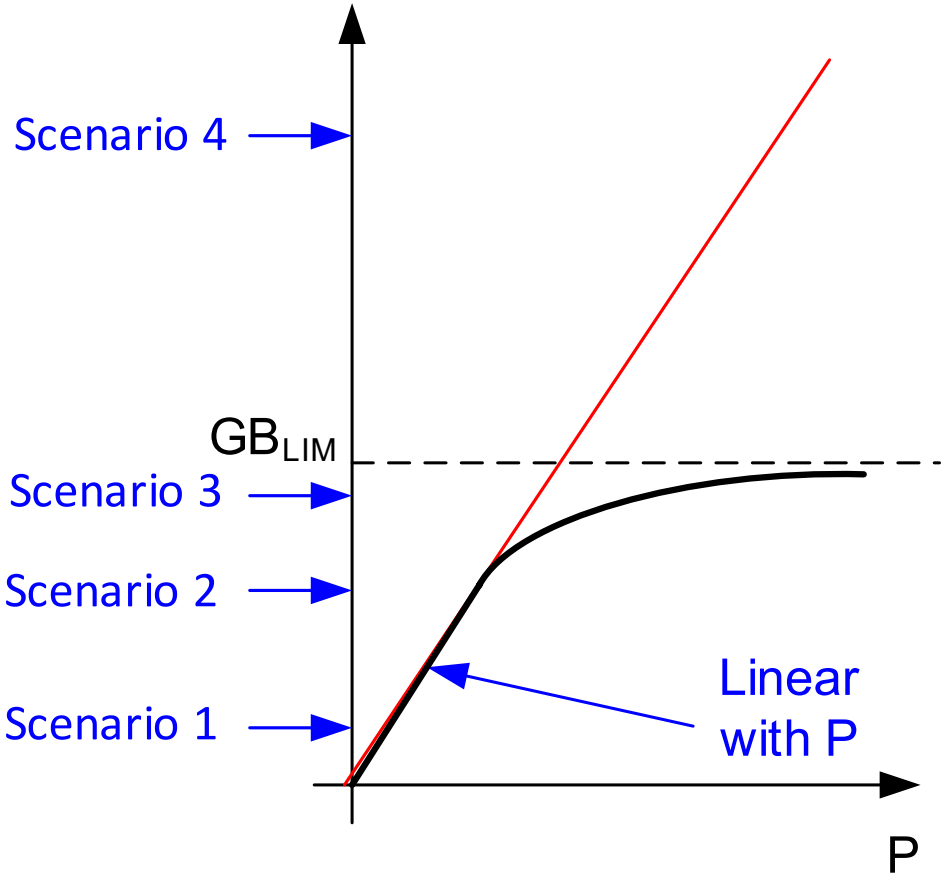
$$P = V_{SUP} \bullet GB \bullet C_L \bullet V_{EB}$$





Interleaving can dramatically reduce power requirements (e.g. two interleaved stages reduce GB requirements a factor of 2 on each stage thereby maintaining power requirements on linear slope region) for high speed data converters but introduces some calibration challenge**s**

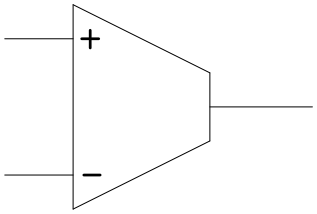
Power Dissipation



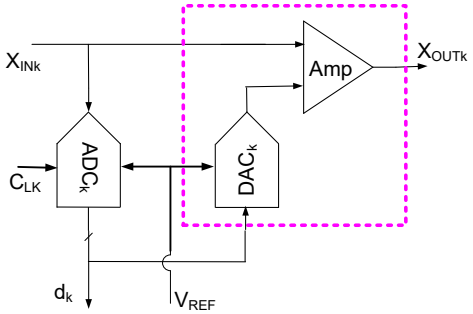
GB$_{LIM}$ strongly technology dependent

What do we do if system requirements are in the respective scenarios?

Power Dissipation



$$GB = \frac{g_m}{C_L}$$



For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

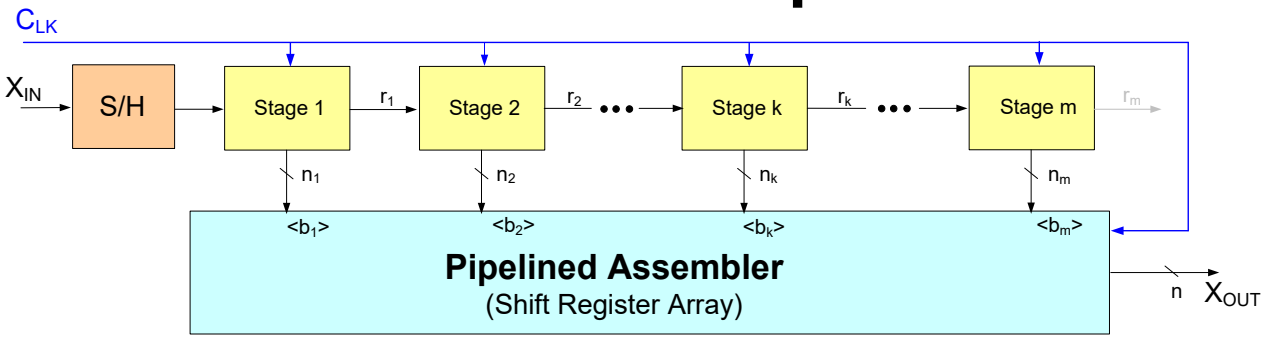
$$P = [V_{SUP} \bullet GB \bullet C_L][V_{EB}]$$

Fixed by ADC requirements

Architecture Dependent

Select architectures that minimize architecture-dependent term

Power Dissipation



For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

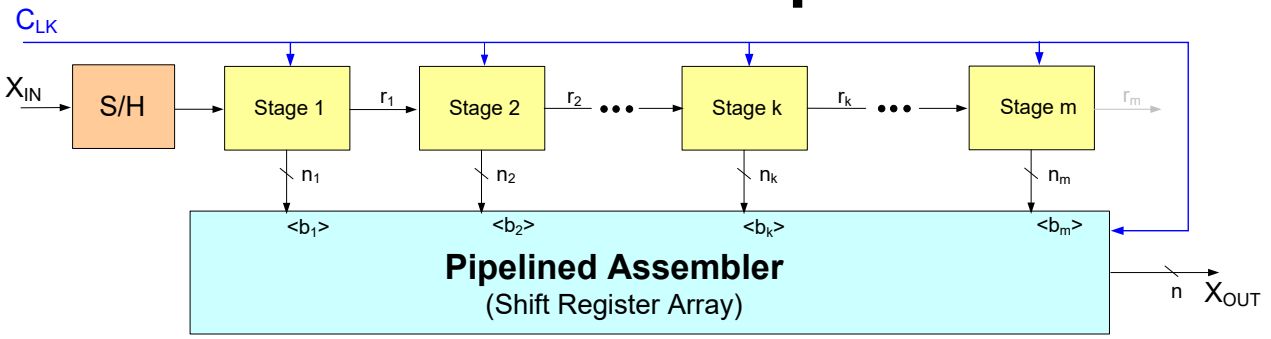
$$P=[V_{SUP} \bullet GB \bullet C_L][V_{EB}]$$

Fixed by ADC requirements

$$GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

- n_{ST}=n for S/H thus S/H is a major power consumer
- Use energy efficient op amp architecture
- Power increases linearly with GB (even faster at high frequencies)
- Interleaving can reduce power dissipation at high frequencies(and extend effective clock speed)
- Power increases linearly with clock speed (or worse at high frequencies)
- Power can be scaled down in latter stages since n_{ST} will decrease
- Amplifiers can be shared between stages or switched off when not used (factor of 2!)
- Using more than one bit/stage will reduce power since no of op amps will decrease (offsets decrease in β)
- Elimination of S/H will have dramatic effect on power reduction

Power Dissipation



For Single-stage MOS implementation (with ref SE op amp or telescopic cascade op amp)

$$P = [V_{SUP} \bullet GB \bullet C_L][V_{EB}]$$

Fixed by ADC requirements

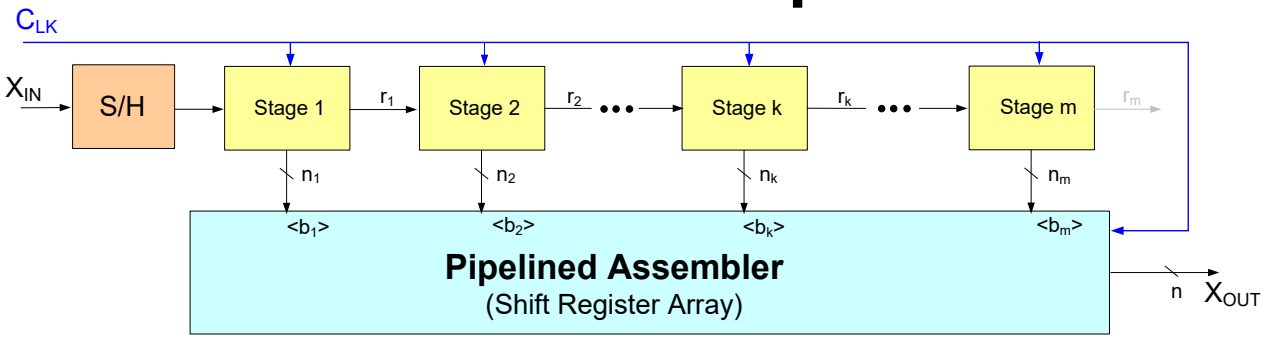
$$GB_{HZ} \cong \frac{0.22(n_{ST}+1)}{\beta} f_{CLK}$$

Which op amp architectures are most energy efficient?

- Depends upon β
- For smaller β, two-stage are more energy efficient for larger β single-stage are better
- Must optimize power in any given architecture
- Folding reduces efficiency (typically by 30% to 50%)

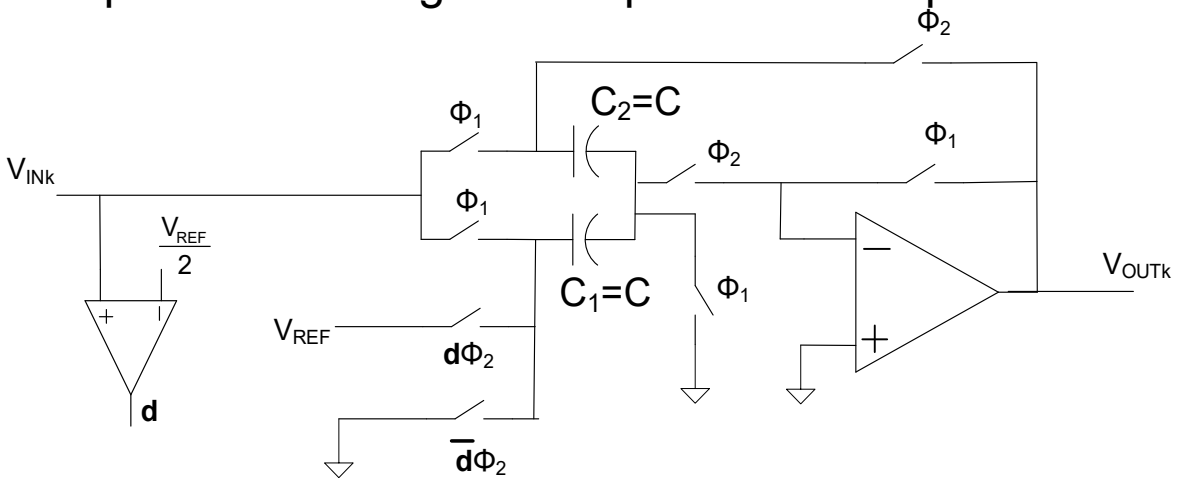
V. Katyal, Y. Lin, and R. L. Geiger, "Power Dependence of Feedback Amplifiers on Op Amp Architecture," *IEEE Int. Symposium on Circuits and Systems*, Kobe, Japan, May 2005, pp. 1618-1621.

Power Dissipation



Capacitor sizing strategies

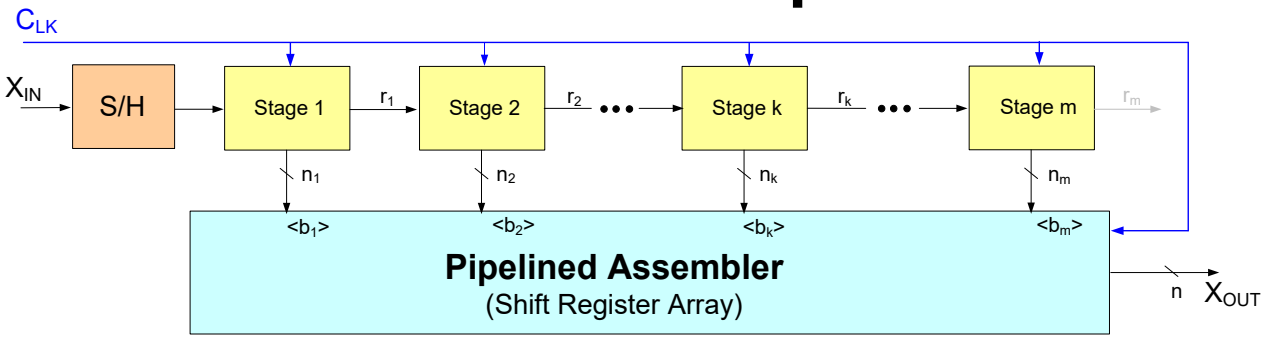
Recall input to each stage is sampled onto a capacitor C



Size of C affects both the noise ($\sqrt{\frac{kT}{C}}$) and gain accuracy

Sampled noise on both C_1 and C_2 appear on output during ϕ_2

Power Dissipation



Capacitor sizing to meet noise requirements

For each stage: $P=[V_{SUP} \bullet GB \bullet C_L][V_{EB}]$

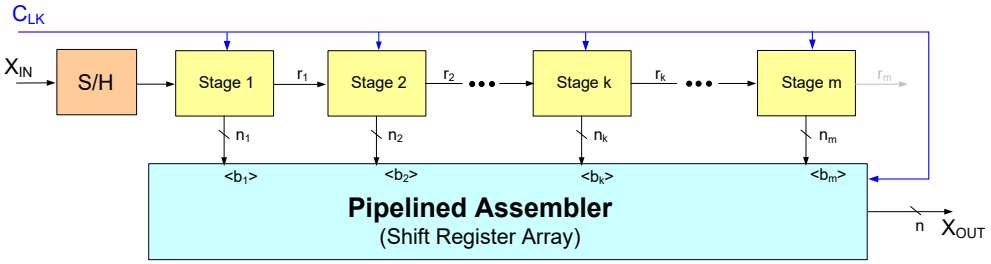
kT/C noise is contributed by each stage

If calibration is used to manage capacitor mismatch, capacitor sizing determined by noise requirements

Should capacitor area be allocated to put dominant noise on input stage or later stages?

If part of the total noise comes from latter stages, size of capacitors on input stage will be increased

Power Dissipation



$$P=[V_{SUP}\bullet GB\bullet C_L][V_{EB}]$$

$$GB_{RPS}\cong\frac{1.4(n_{ST}+1)}{\beta}f_{CLK}$$

$$P=\left[V_{SUP}\frac{1.4}{\beta}f_{CLK}V_{EB}\right]C_L(n_{ST}+1)$$

$$P=X_F(n_{ST}+1)C_L$$

Example: How do the op amp power requirements change from one-stage to the next with two bits per stage in a 16-bit pipeline. Assume a charge-redistribution gain stage and the size of the capacitors are scaled to keep the noise contributions the same in each stage. Assume the first stage has a total sampling capacitor of value C_1 and all noise is captured on input samples for each stage

Will keep the dc op amp gain for each stage the same

$$V_{n1}=\sqrt{\frac{kT}{C_1}}$$

$$V_{n2}=\sqrt{\frac{kT}{C_2}}$$

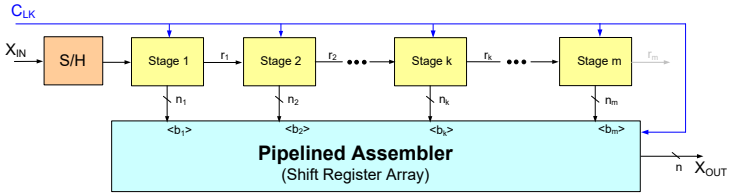
$$V_{n2}=4V_{n1}$$

$$C_2=\frac{C_1}{16}$$

$$P_1=X_F(14+1)C_{L1}$$

$$P_2=X_F(12+1)\frac{1}{16}C_{L1}\cong 0.05\bullet P_1$$

Power Dissipation



Example sol continued:

$$P_1 = X_F (14+1) C_{L1}$$

$$P_2 = X_F (12+1) \frac{1}{16} C_{L1}$$

$$P_3 = X_F (10+1) \frac{1}{16^2} C_{L1}$$

$$P_4 = X_F (8+1) \frac{1}{16^3} C_{L1}$$

$$P_5 = X_F (6+1) \frac{1}{16^4} C_{L1}$$

$$P_6 = X_F (4+1) \frac{1}{16^5} C_{L1}$$

$$P_7 = X_F (2+1) \frac{1}{16^6} C_{L1}$$

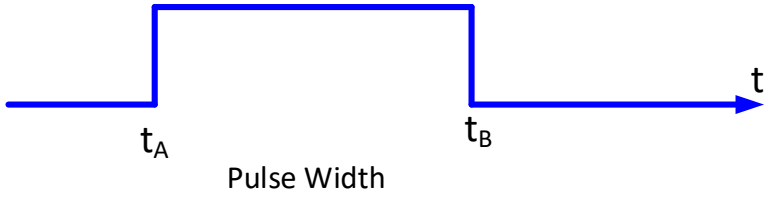
- Power completely dominated by first stage
- Will likely not scale C so much so noise will be dominated by first stage
- No benefit from scaling power in latter stages

Pipelined Data Converter Design Guidelines

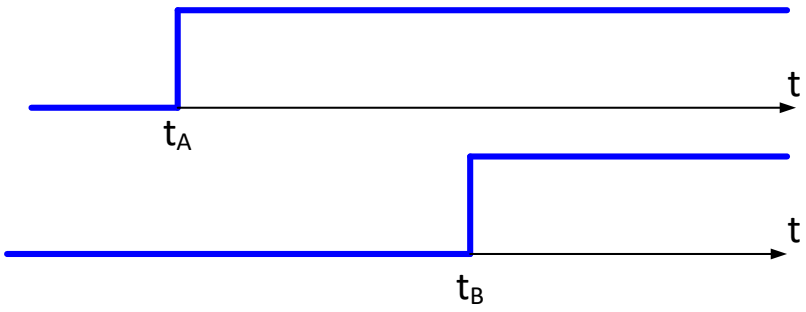
	Issue		Strategy
1.	ADC offsets, Amp Offsets, Finite Op Amp Gain, DAC errors, Finite Gain Errors all cause amplifiers to saturate	1.	Out-range protection circuitry will remove this problem and can make pipeline robust to these effects if α_k's correctly interpreted a) Use Extra Comparators b) Use sub-radix structures
2.	Op Amp Gain causes finite gain errors and introduces noninearity	2.	a) Select op amp architecture that has acceptable signal swing b) Select gain large enough at boundary of range to minimize nonlinearity and gain errors
3.	Op amp settling must can cause errors	3.	Select GB to meet settling requirements (degrade modestly to account for slewing)
4.	Power dissipation strongly dependent upon GB of Op Amps	4.	Minimize C_L, use energy efficient op amps, share or shut down op amp when not used, scale power in latter stages, eliminate input S/H if possible, interleave at high frequencies. Good (near optimal) noise distribution strategy should be followed.

Time to Digital Converters (TDC)

(technically tDC since TDC often refers to Temp to Digital Converter)



Pulse Width



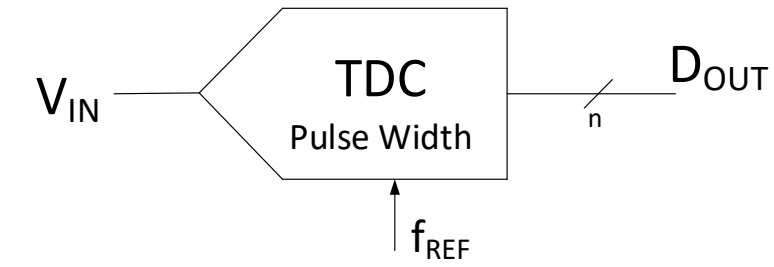
Time Interval

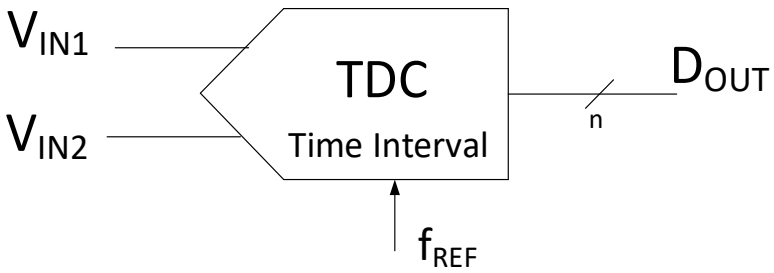
Both Pulse Width and Time Interval Requirements

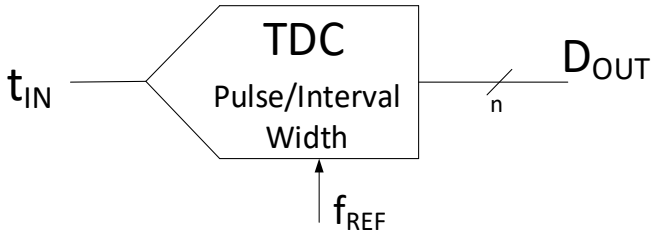
Time to Digital Converters (TDC)

(technically tDC since TDC often refers to Temp to Digital Converter)

Time input is width of Pulse or Interval between "voltage" inputs indicated in figure







Both Are Used

Time to Digital Converters (TDC)

Applications:

Time of Flight (LIDAR, SONAR,RADAR)

Flow Meters

Chemical Reaction Times

Atomic collisions

Temperature Sensors

Alternative to Voltage Mode Data Conversion

Time to Digital Converters (TDC)

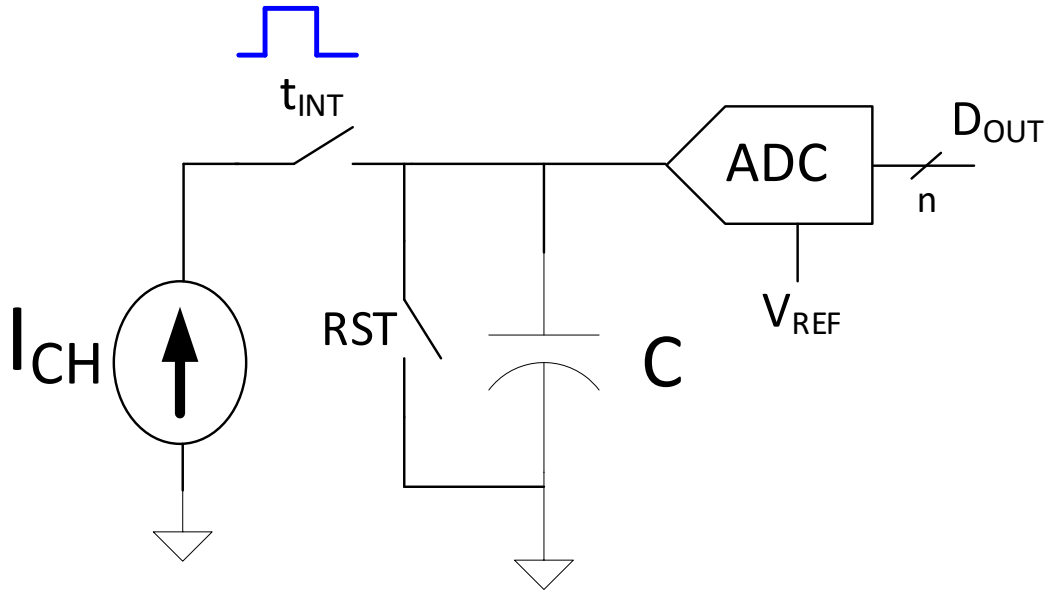
Alternative to Voltage Mode Data Conversion

- Convert Analog Voltage to Pulse Width or Time Interval
- Use TDC to obtain Digital Output

Some argue that with decreasing supply voltage, voltage headroom is inherently limited but there is no fundamental limit in headroom or resolution when operating in the time domain

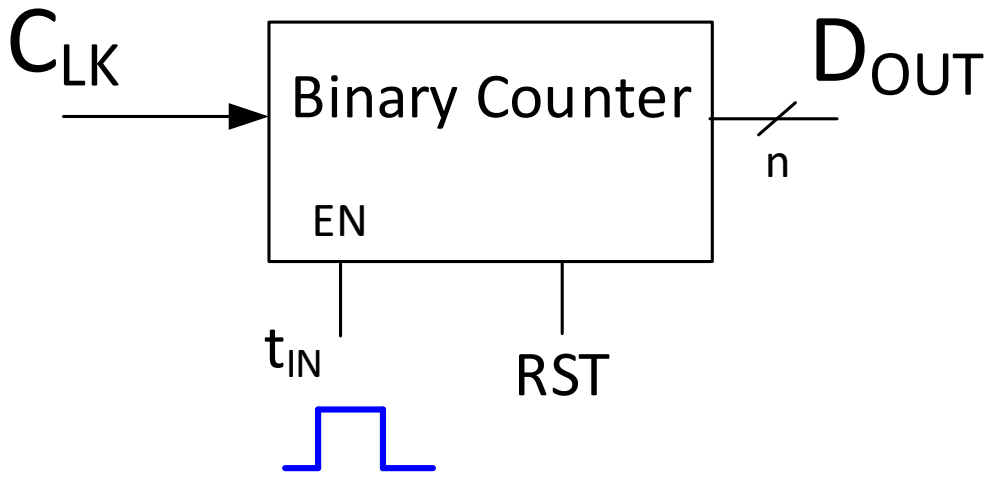
This is not the primary use of TDC today but is receiving some interest

One Basic Concept of a TDC



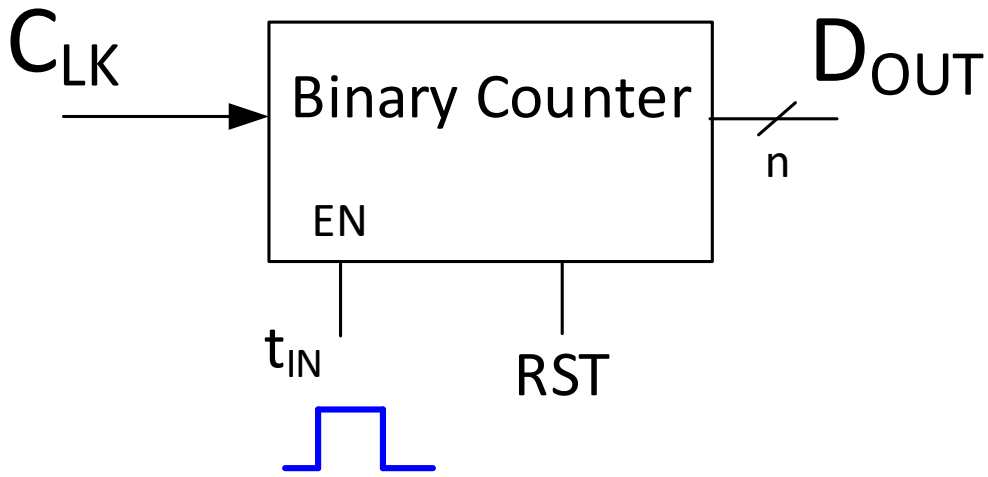
- Simple
- Modestly Accurate
- Slow

Another Basic Concept of a TDC



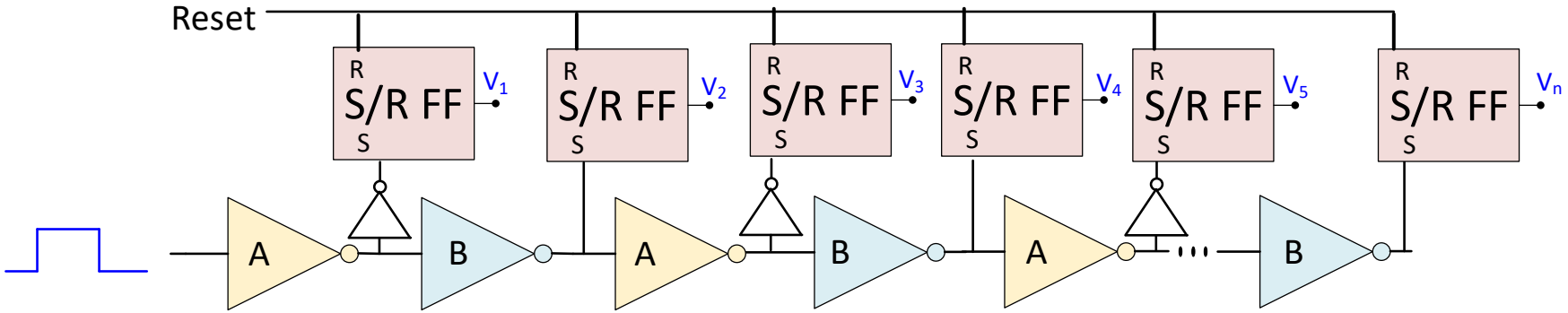
- Simple
- Accurate
- Slow

Another Basic Concept of a TDC



- Simple
- Accurate
- Slow

Vernier Delay Line Approach to TDC



By appropriately setting delays in alternating two types of delay stages, pulse will disappear someplace in delay line

After pulse disappears, pulse width will be encoded in the thermometer code that appears in $<V_1,V_2,.....V_n>$

Delay stages can be designed to shrink (or stretch) pulse by same amount in each stage

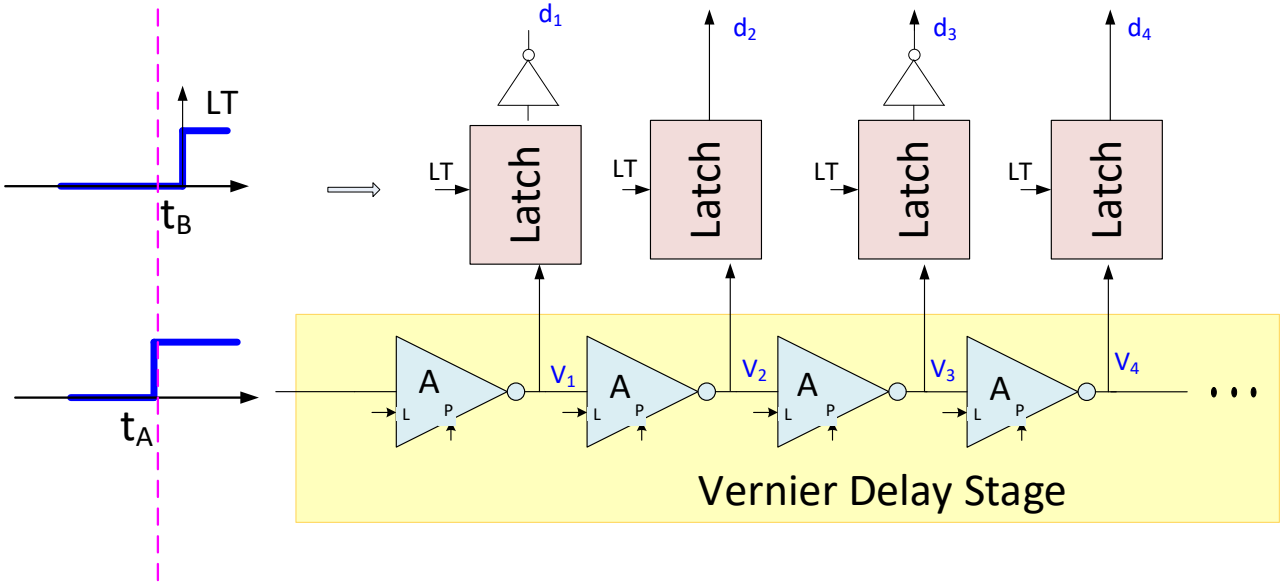
Very fine resolution in pulse shrink (or stretch) rate can be achieved by appropriate sizing of delay stages

If delay stages are programmable (discussed later) total delay can be accurately calibrated with f_{REF}

Large number of stages needed for high resolution

INL degrades with mismatch in delay elements

Vernier Delay Line Approach



Latch outputs determine how far input pulse propagated before arrival of t_B

Thermometer Code in Latch Outputs must be decoded

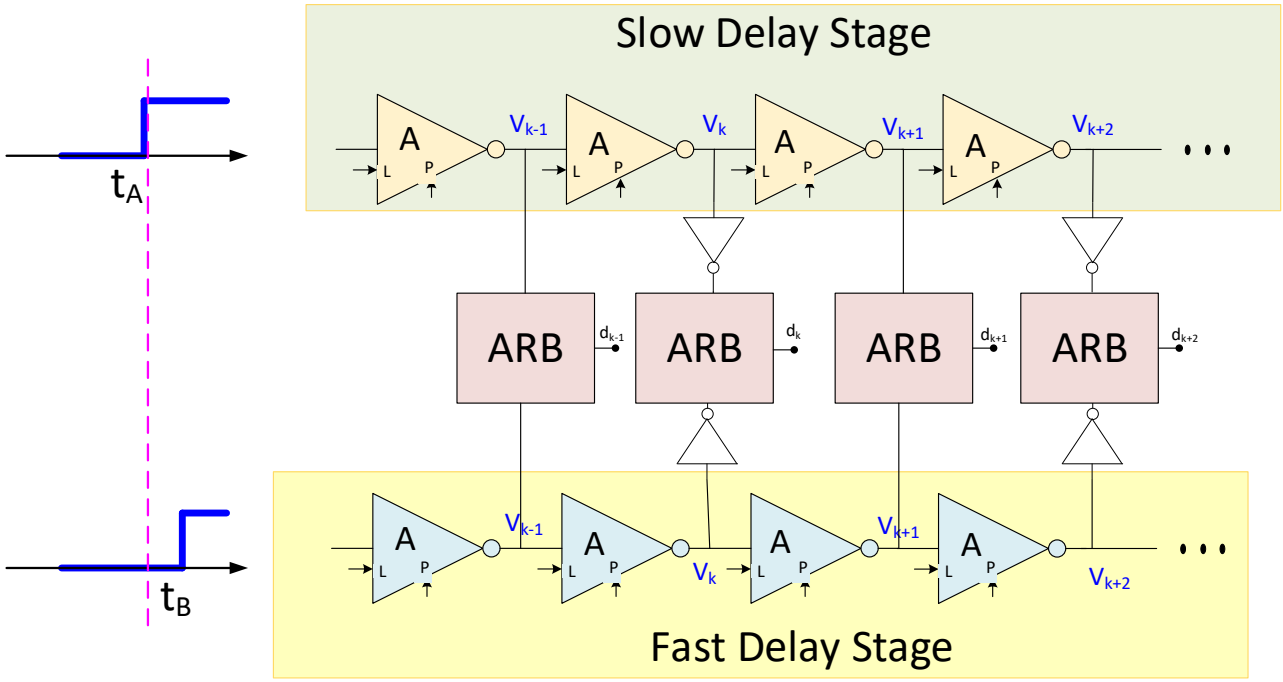
Large number of delay stages for high resolution

INL degrades with mismatch in delay elements

Resolution limited by delay of delay elements

Calibration with known time reference needed for reasonable accuracy

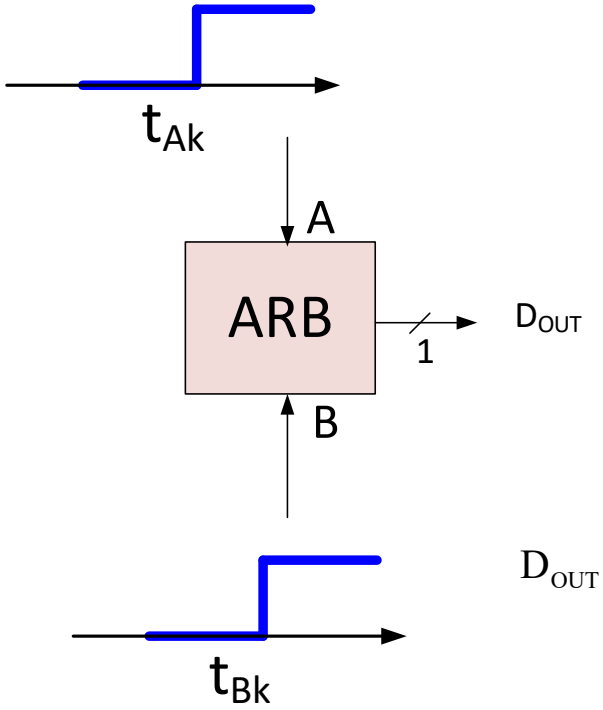
Dual Vernier Delay Line Approach



Delayed pulse in fast delay line “catches up” with pulse in slow line
Arbiter determines which pulse arrives first
Time difference thermometer coded in ARB outputs
Very fine resolution is $\delta_A=\delta_B+\varepsilon$ when ε is very small
Useful for measuring very short pulses
Number of stages gets large for high resolution
Nonlinearity due to random variations in delay stages

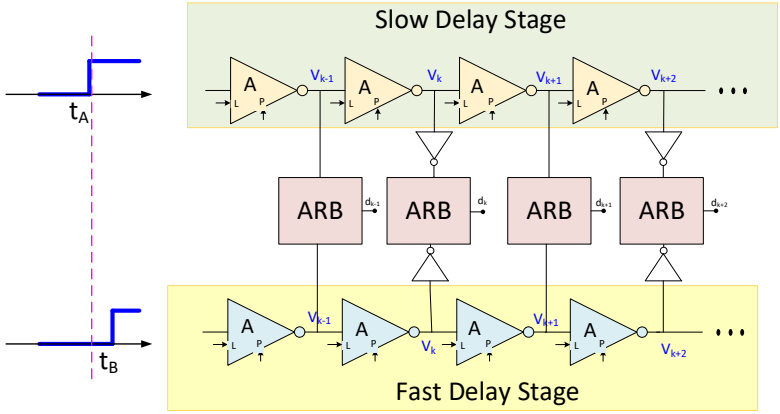
Dual Vernier Delay Line Approach

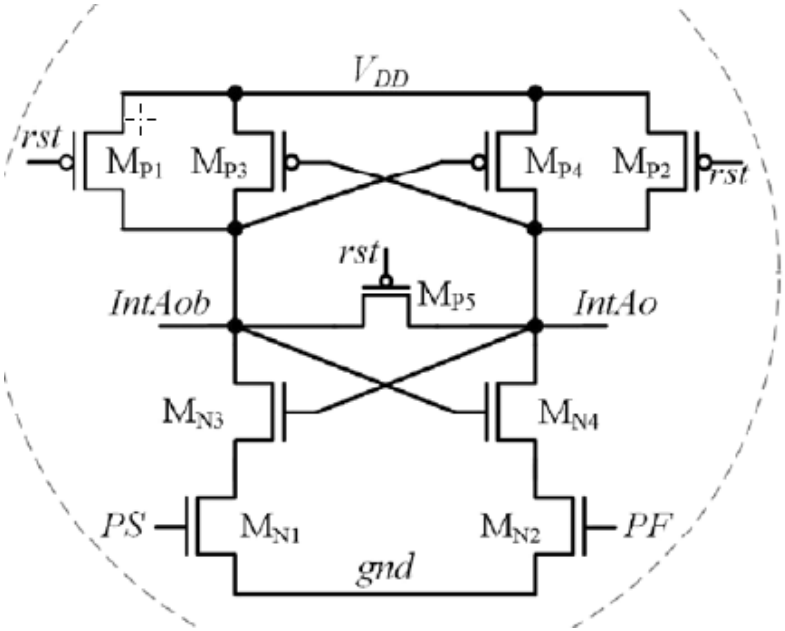
Arbiter



$$D_{OUT} = \begin{cases} 0 & \text{If pulse A arrives first} \\ 1 & \text{If pulse B arrives first} \end{cases}$$

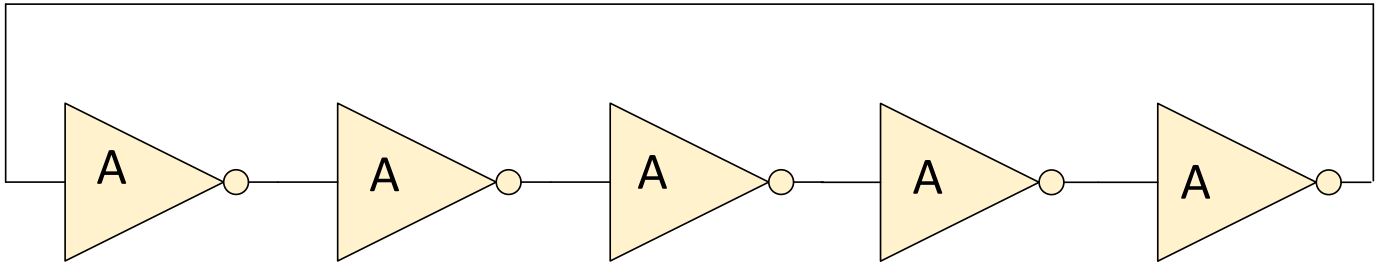
Dual Vernier Delay Line Approach



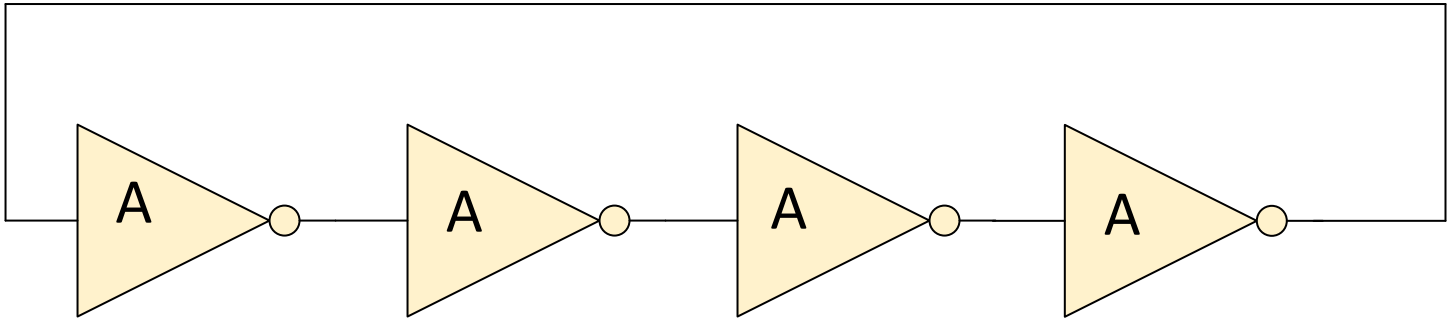


One Arbiter Circuit

Pulse Shrinking TDCs



Odd number of delay elements in loop

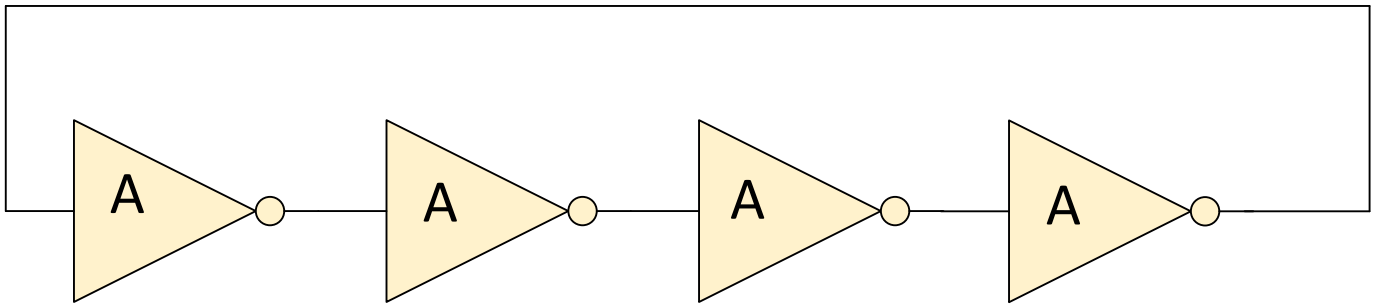


Even number of delay elements in loop

Odd number of inverting delay elements forms a Ring Oscillator $f_{OSC} \simeq \frac{1}{n\left(t_{HL}+t_{LH}\right)}$

Even number of delay elements forms, in steady state,
a latch with alternating <0 1 0 1…> or <1 0 1 0 …>

Pulse Shrinking TDCs



Even number of delay elements in loop

<0 1 0 1…> or <1 0 1 0 …>

Odd number of inverting delay elements has received little attention (boring !)

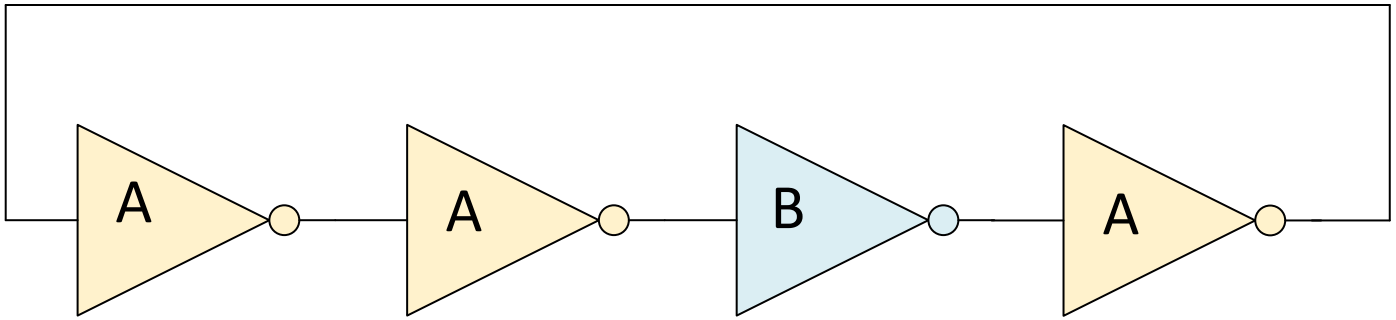
But, it can be shown that if the delay elements are matched and a pulse is inserted into the loop, the pulse will circulate indefinitely !

Actually two or more pulses could circulate as well if there are a sufficient number of delay stages!

But even if the delay stages are ideally identical, random variations in delay characteristics will cause the a pulse to either stretch or shrink thus eventually causing the outputs to enter one of the two static Boolean states

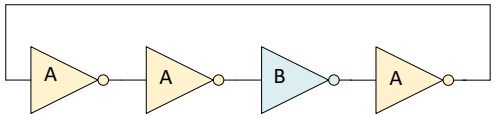
Is there any practical use of this unique pulse-shrinking or pulse-stretching feature?

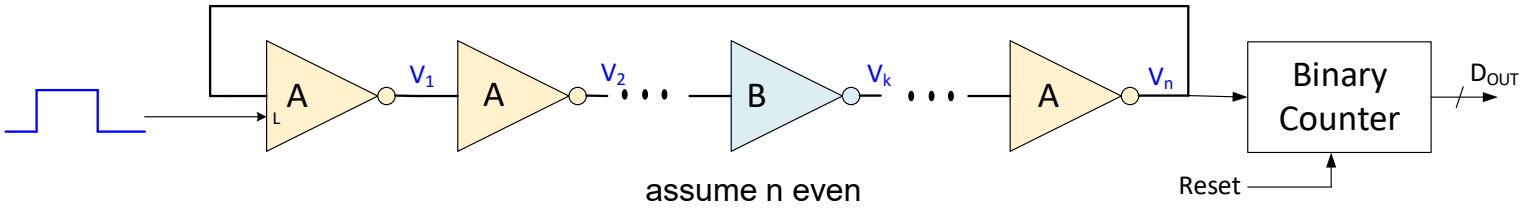
Pulse Shrinking TDCs



It can be shown that if a single delay element has different total propagation delays than the remaining elements, then a pulse inserted in the ring of an even number of inverting stages will stretch or shrink by precisely the same amount every time the pulse traverses the loop until it ultimately disappears and the stretch/shrink rate can be accurately controlled by judicious design of the delay stages.

Pulse Shrinking TDCs





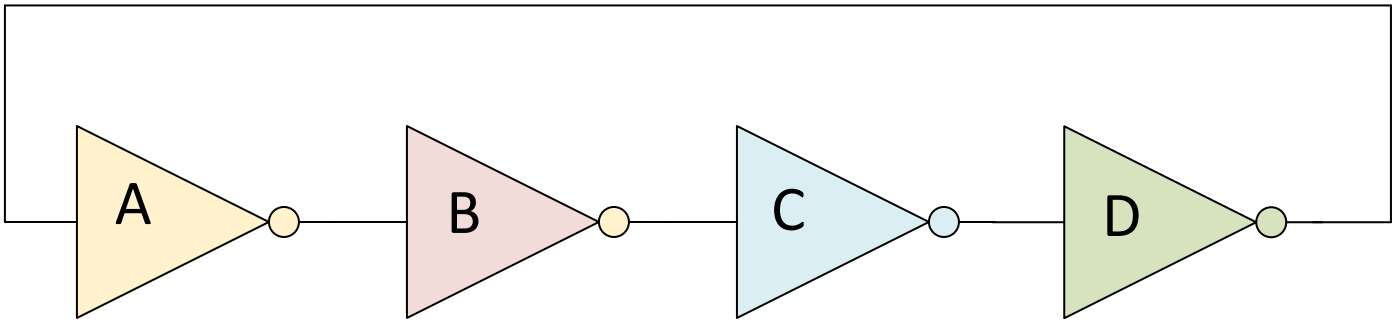
Insert single “inhomogeneous” delay stage that causes pulse to shrink

Forms TDC with output in the Binary Counter after pulse disappears

Resolution can be very high by making difference between A and B delays very small

In contrast to Vernier approaches where random variations in delay cause INL errors, INL is very small since same elements are used for delay shrink each time pulse goes around loop

Pulse Altering Even-Order Delay Rings

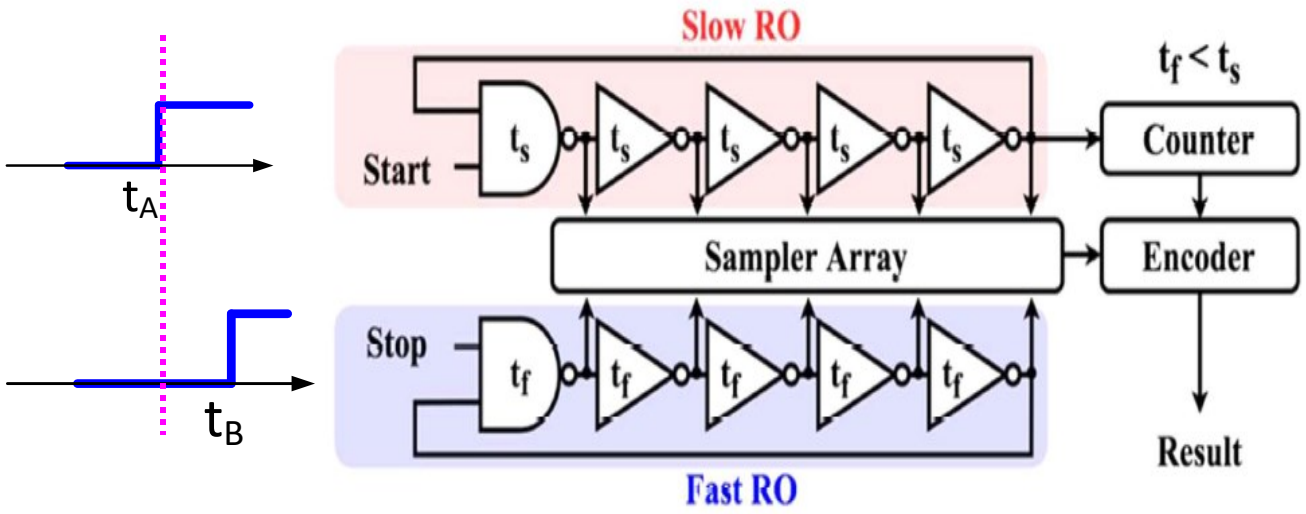


These structures have received minimal attention in the research community

Maybe they should be considered as a fundamental circuit structure that likely has a multitude of applications

Even some of the most basic properties of these structures have not been explored !

Gated Dual Vernier Delay Line TDC



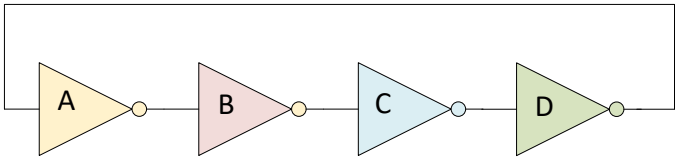
Uses “gated” Ring Oscillators

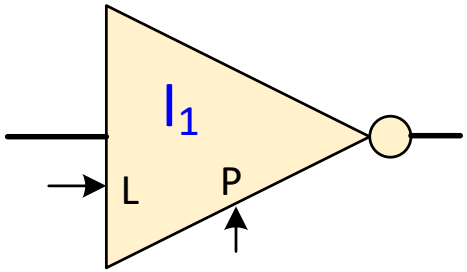
Sampling array is an array of Arbiters

Claim high resolution is possible

Mismatch in delays introduce INL errors

Pulse Altering Even-Order Delay Rings



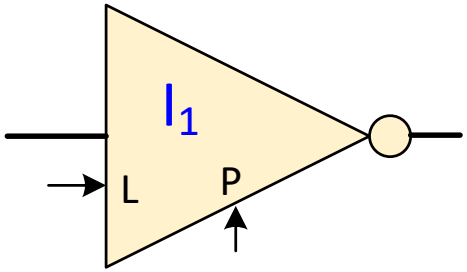


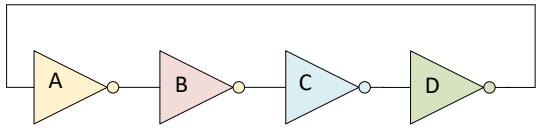
Generic Inverting Delay State

- Input Port
- Output Port
- Load Port
- Program/Cal Port (optional)

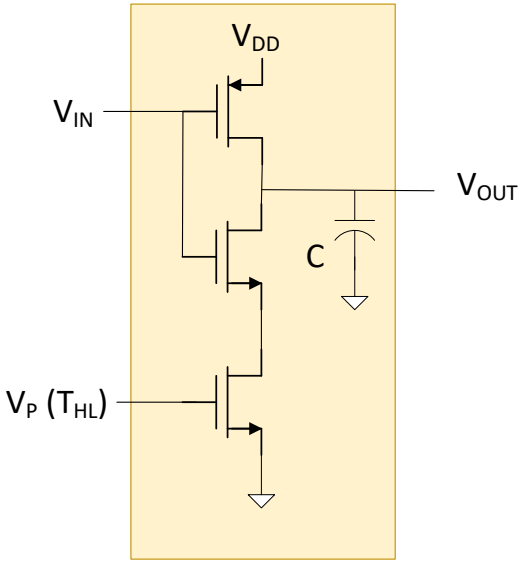
Concept of Pulse Altering Circuit Applicable to Wide Array of Delay Stages

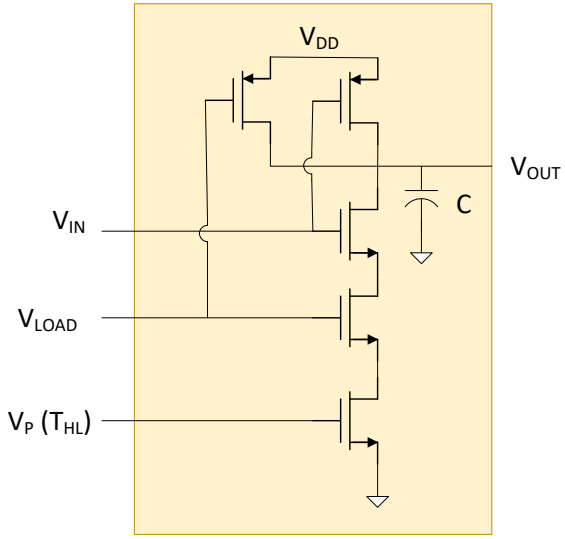
Pulse Altering Even-Order Delay Rings

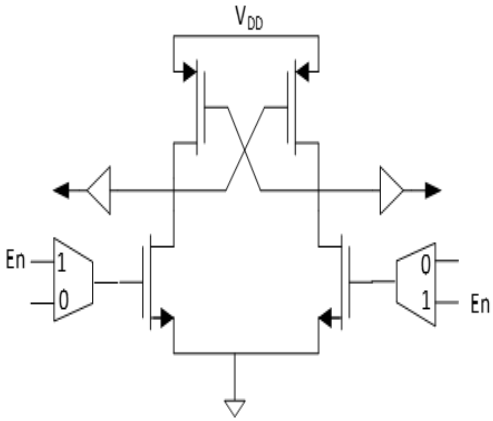




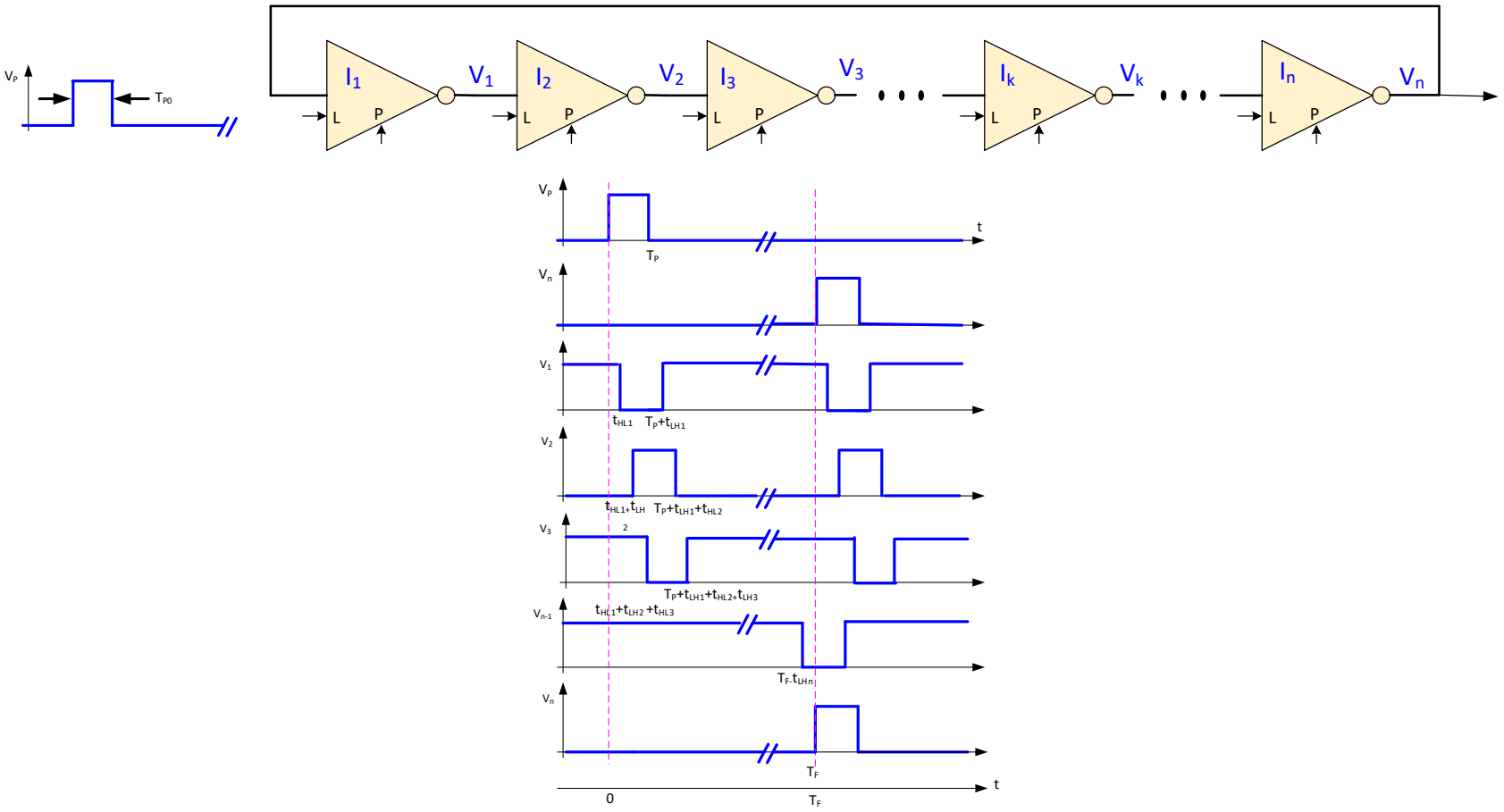
Some Reported Delay Cells







Pulse Altering Even-Order Delay Rings

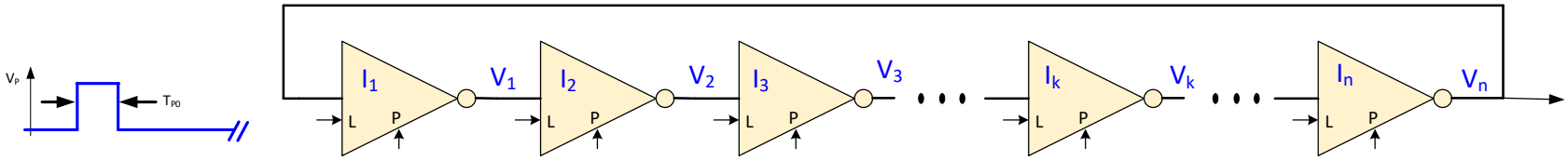


t_{SRK} is the amount of shrink for pulse looping once (independent of how often pulse loops)

$$t_{SRK} = T_{P1} - T_{P0} = t_{LH1} + t_{HL2} + t_{LH3} + \ldots\ldots + t_{HLn} - t_{HL1} - t_{LH2} - t_{HL3} - \ldots\ldots - t_{LHn}$$

Pulse Altering Even-Order Delay Rings

Special Case 1 Even number of Identical Stages



$$t_{SRK} = T_{P1} - T_{P0} = t_{LH1} + t_{HL2} + t_{LH3} + \ldots\ldots + t_{HLn} - t_{HL1} - t_{LH2} - t_{HL3} - \ldots\ldots - t_{LHn}$$

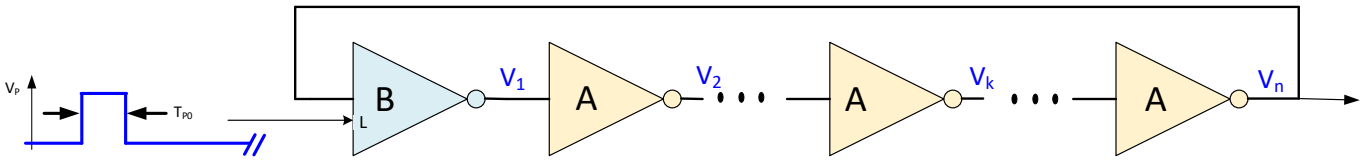
Regrouping

$$t_{SRK} = t_{LH1} - t_{HL1} + t_{HL2} - t_{LH2} + t_{LH3} - t_{HL3} + \cdots\ldots + t_{HLn} - t_{LHn}$$

If matched, t_{SRK}=0 so pulse circulated indefinitely

Pulse Altering Even-Order Delay Rings

Special Case 2 Even number of with single mismatched on Stage 1



t_{SRK} is the amount of shrink for pulse looping once

$$t_{SRK} = T_{P1} - T_{P0} = t_{LH1} + t_{HL2} + t_{LH3} + \ldots\ldots + t_{HLn} - t_{HL1} - t_{LH2} - t_{HL3} - \ldots\ldots - t_{LHn}$$

$$t_{SRK} = \delta_{LH1} + t_{LHN} + (-t_{HLN} - \delta_{HL1} + t_{HLN}) + (-t_{LHN} + t_{LHN}) + (-t_{HLN} + t_{HLN}) \ldots\ldots (-t_{HLN} + t_{HLN}) - t_{LHN}$$

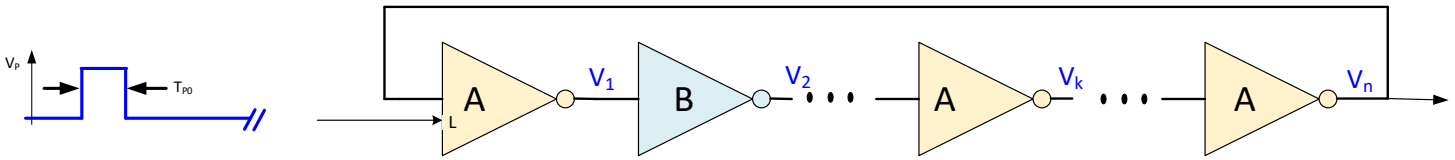
This simplifies to

$$t_{SRK} = \delta_{LH1} - \delta_{HL1}.$$

pulse shrinks (if $t_{SRK}<0$) or grows (if $t_{SRK}>0$)

Pulse Altering Even-Order Delay Rings

Special Case 3 Even number of with single mismatched on Stage 2



t_{SRK} is the amount of shrink for pulse looping once

$$t_{SRK} = T_{P1} - T_{P0} = t_{LH1} + t_{HL2} + t_{LH3} + \ldots\ldots + t_{HLn} - t_{HL1} - t_{LH2} - t_{HL3} - \ldots\ldots - t_{LHn}$$

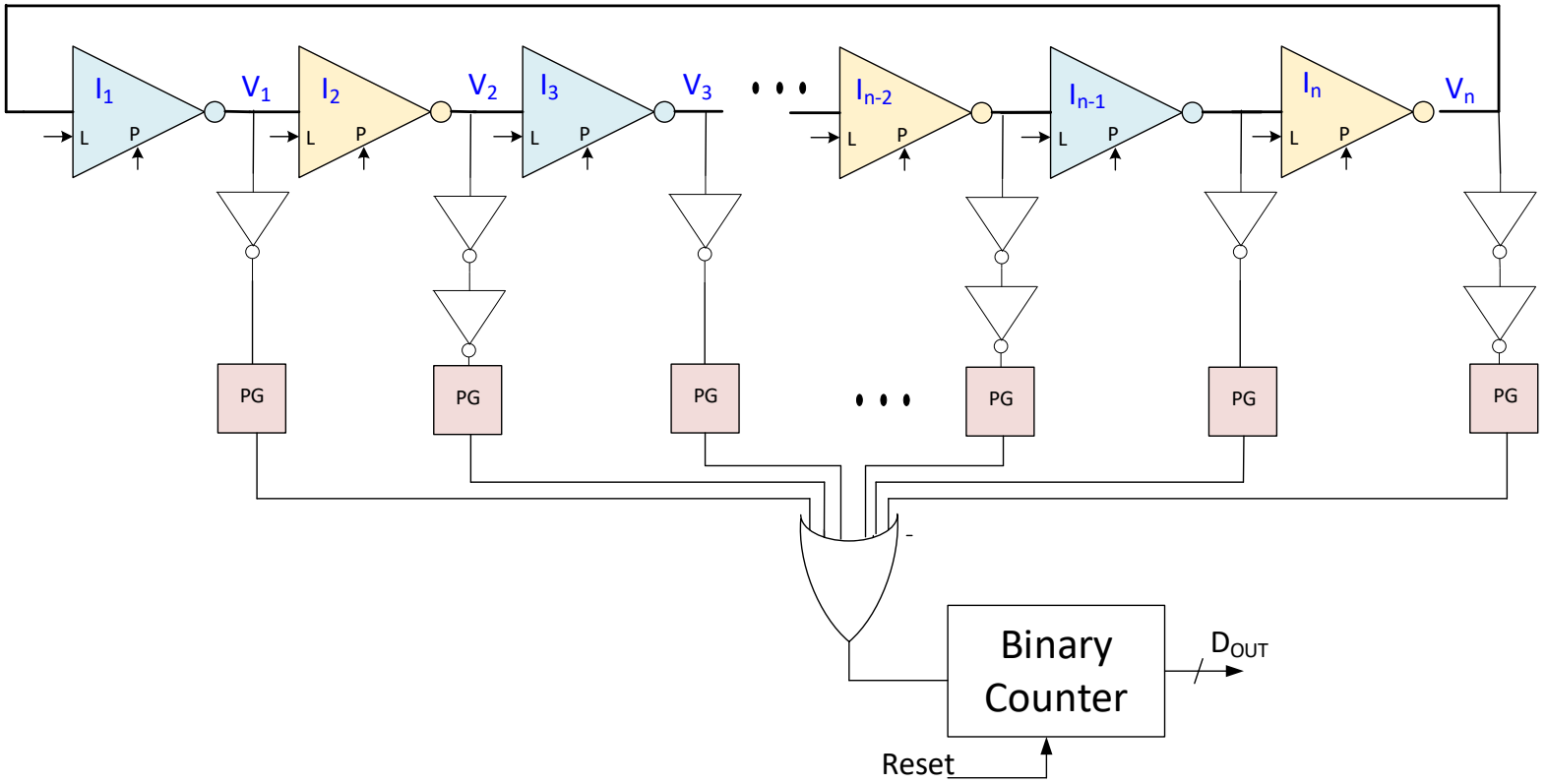
$$t_{SRK} = t_{LHN} + (-t_{HLN} + t_{HLN} + \delta_{HL2}) + (-t_{LHN} - \delta_{LH2} + t_{LHN}) + (-t_{HLN} + t_{HLN}) \ldots\ldots (-t_{HLN} + t_{HLN}) - t_{LHN}$$

This simplifies to

$$t_{SRK} = \delta_{HL2} - \delta_{LH2}.$$

This is the negative of Special Case 2 ! So if pulse shrinks when in position 1 it will grow when in position 2

A new TDC based upon Pulse Shrinking Rings



Good INL since MSB determined by identical delay elements
Vernier Delay Lines used to Enhance Resolution but Affect only LSB

Stay Safe and Stay Healthy !

End of Lecture 24